REMARKS

The Examiner's Action mailed on June 24, 2009, has been received and its contents carefully considered. It is respectfully requested that this Amendment be entered after final rejection under 37 CFR §1.116(b)(2) as placing the application in better form for consideration on appeal.

In this Amendment, Applicant has amended claim 1. Claim 1 is the sole independent claim pending and under consideration, and claims 1, 2 and 4 remain pending and under consideration in the application, claims 3 and 5-17 having been previously withdrawn in response to the Restriction Requirement of November 3, 2008, although claim 3 has been deemed by the Examiner to be directed merely to a different species of the elected invention, and is thus subject to possible rejoinder. For at least the following reasons, it is submitted that this application is in condition for allowance.

Claims 1-4 were rejected under 35 USC §103(a) as obvious over the combination of *Hirota* (JP 06-268162 A) in view of *Jeng et al.* (US 6,136,643). Please note that the Office Action refers to the primary reference as Yoshihiro, but this appears to be a given name, and Hirota the surname. This rejection is respectfully traversed.

Hirota discloses a semiconductor device having an ordinary-breakdown-strength MOS transistor **30** and a high-breakdown-strength MOS transistor **11** both formed on a semiconductor substrate **10**. However, a LOCOS isolation

structure using a field oxide film **33** is applied to both the regions around the ordinary-breakdown-strength MOS transistor **30** and around the high-breakdown-strength MOS transistor **11**.

According to the present invention, on the other hand, an STI (Shallow Trench Isolation) structure is adopted for the first region including the device with the lower breakdown voltage, while a LOCOS structure is adopted for the second region including the device having the higher breakdown voltage. Thus, the present invention is structurally different from *Hirota*. See the present specification as filed, e.g. ¶¶[0036] and [0069]:

> **[0001]** With this arrangement, so-called shallow trench isolation (STI) is employed for the device isolation in the first region formed with the first device of the lower breakdown voltage, so that the microminiaturization of the structure in the first region can be advantageously achieved. On the other hand, the second device of the higher breakdown voltage formed in the second region has the drift drain structure with the LOCOS oxide film provided at the edge of the gate electrode, so that the problem of the concentration of the electric field can be suppressed which may otherwise occur when a thick insulation film of an STI portion is disposed on the edge of the gate electrode. Thus, the second device has a sufficient breakdown voltage.
>
> **[0002]** The lower breakdown voltage transistors **51** formed in the first region **50** are respectively disposed in device formation regions **53** isolated by a shallow trench isolation (STI) portion **52** formed in a surface of the silicon substrate **40**. The STI portion **52** is formed by filling silicon oxide **55** in a shallow trench **54** (e.g, having a depth of about 4000Å) formed in the surface of the semiconductor substrate **40**.

In the STI portion of the structure of the present invention, the surface of the device isolation portion and the surface of the semiconductor substrate are flush with each other, i.e., the surfaces are in the same plane.

The structure of the device according to *Hirota* is shown in Drawing 1 thereof, from which it is apparent that the field oxide film **33** is not flush with a surface of the substrate, but instead stands proud therefrom, i.e. the field oxide film **33** does not have a surface in a common plane with a surface of the substrate. This follows directly because the field oxide film **33** has been made by local oxidation, i.e. by a LOCOS process, and not by filling a trench, whereas in the present invention the device isolation portion is made by filling a trench until it is flush with the substrate.

Hirota (Yoshihiro) thus fails to disclose a structure in which an STI structure is adopted for a first region while a LOCOS structure is adopted for a second region.

The Office Action states on page 3 thereof that *Jeng et al.* discloses "Wherein a surface of the device isolation portion and a surface of the semiconductor substrate are both arranged in a common plane" in column 2, lines 35-46 thereof:

> ... This allows self-aligned contacts to be made with relaxed photolithographic alignment tolerances.
>
> The method begins by providing a semiconductor substrate. Typically the substrate is a P^- doped single-crystal silicon substrate having a <100> crystallographic orientation. Device areas are provided by forming a relatively thick Field OXide (FOX) that surrounds and electrically isolates each device area in and on the substrate. One method of forming the field oxide is by shallow trench isolation (STI) in which a shallow trench is etched in the substrate and filled with a silicon oxide (SiO_2) that is made essentially planar with the substrate surface. ...

Thus, *Jeng et al.* discloses an STI structure. However, *Jeng et al.* fails to teach or suggest a structure that includes within it both an STI structure and a LOCOS structure.

As *Hirota* (Yoshihiro) and *Jeng et al.* both fail to teach or suggest a structure that includes an STI structure in a first region and a LOCOS structure in a second region, they must naturally fail to teach or suggest a structure in which an insulator for the STI structure is continuous with a LOCOS oxide film at a boundary between the first and second regions.

That is to say, neither *Hirota* (Yoshihiro) nor *Jeng et al.*, whether taken separately or in combination, teaches or suggests "wherein the insulator of the device isolation portion and the LOCOS oxide film are continuous at a boundary between the first region and the second region" as recited in claim 1.

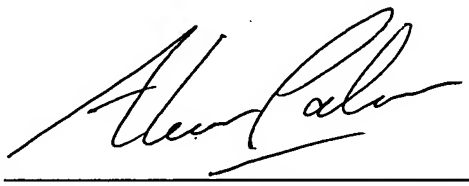
Consequently, claim 1 patentably defines over *Hirota* (Yoshihiro) and *Jeng et al.* and is allowable, together with claims 2 and 4 dependent therefrom, and as claim 1 is generic it is respectfully requested that the species of withdrawn claim 3 be rejoined with the species of claims 2 and 4, and claim 3 allowed therewith.

It is submitted that this application is in condition for allowance. Such action and the passing of this case to issue are requested.

Should the Examiner feel that a conference would help to expedite the prosecution of this application, the Examiner is hereby invited to contact the undersigned counsel to arrange for such an interview.

No remittance is believed to be due. Should any fee be required, however, the Commissioner is hereby authorized to charge the fee to our Deposit Account No. 18-0002, and advise us accordingly.

Respectfully submitted,



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Date

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